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10/591,178	08/30/2006	Pierre Blanchard	4590-556	7764

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EXAMINER	
GUMEDZOE, PENIEL M	
ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,178	BLANCHARD, PIERRE	
	Examiner	Art Unit	
	PENIEL M. GUMEDZOE	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/03/08, has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites “reading diode”, “electrodes”, silicon layer”. It is unclear from the specifications and drawings, what those words referrer to in the claim. There is no recitation of “reading diode” preceding the first appearance of the expression “the reading diode” and it is unclear if this element is the same as the “readout diode”. It is also unclear from the drawing how the readout diode (DL) is delimited on one side by the electrodes and on the other side by regions of thick silicon oxide. It appears to Examiner that the reading diode is instead delimited on two sides by the electrodes

(reset and last), and on the remaining other sides by regions of thick oxide (fig. 2). Finally, There is no recitation of "silicon layer" preceding the first appearance of the expression "the silicon layer" and it is unclear if this element is the same as the "polycrystalline silicon".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565) and further in view of Kub ('604).

Kamimura et al. ('565) disclose a method for fabricating a CCD shift register having electrodes (fig. 1, col. 2. ln. 43-44) comprising: producing (this is implicit since if the electrodes are in the structure, they have been produced to be there) a last electrode of the shift register (see electrode 5a on the right side of fig. 1 and note that since the structure repeats (see col. 2 ln 41) in a finite manner, there would be a point where such an electrode would be a last electrode regardless of what is made beyond it), and a reset electrode (see electrode 5a&5b directly on the left of the last electrode as previously defined on fig. 1), separated by a gap above a substrate (see fig. 1); exposing the surface of the substrate (col. 2 ln. 48-50); depositing a layer of doped polycrystalline silicon 7 entering in contact with the substrate in order to form one pole

of a diode, the substrate forming another pole (col. 2 ln. 50-54); partially removing the polycrystalline silicon while leaving a desired pattern (independent sections of 7) covering at least a space left between said last electrode and said reset electrode and also covering a region lying outside the space (see fig. 1 and col. 2 ln. 50-58 noting that it is implicit that the polysilicon 7 has been selectively removed in order to obtain the gap between the independent sections of 7 shown on fig. 1); depositing an insulating layer 8 above the polycrystalline silicon and locally etching an opening in the insulating layer outside the space lying between the electrodes (fig. 1, col. 2 ln. 54-60), depositing and etching a metal layer 9 to form a contact with the polycrystalline through the opening (Fig. 1, col. 2 ln. 58-63). But Kamimura et al. ('565) do not appear to explicitly disclose silicon electrodes and thermally oxidizing the said electrodes to form the electrodes' insulating layers.

However Kub ('604) discloses silicon electrodes and oxidizing said electrodes in height and width (it is inherent that the oxidation would also occur in width) to form insulating layers, leaving a space between said electrodes in order to define a doped (contact) layer of a CCD diode (see Fig.2 and column 5 lines 55-68 of '604).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have formed polysilicon electrodes (the use of silicon electrode in CCD is well known in the art (see for example fig. 8, [0162] of '075 cited in previous office action as well as Kub '064), and as such, the use of conventional materials/components is obvious (see MPEP 2144.07)) and oxidized them to form the

insulating film 6 of the device of '565 in order to define the doped region 2 of the diode of the CCD structure.

Alternatively, it would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have formed silicon electrodes (the use of silicon electrode in CCD is well known in the art (see for example fig. 8, [0162] of '075 cited in previous office action as well as Kub '064), and as such, the use of conventional materials/components is obvious (see MPEP 2144.07)) according to Kub ('064) in order to avoid the multiple steps of forming the silicon dioxide layer 6 (see fig. 1 of '565 noting that layer 6 entirely covers and extends between 5a and 5b as well as between 5a and the substrate) that would cover the electrodes since there would have been the need of forming a first oxide layer on the substrate before forming electrode 5a, then forming another layer of oxide to cover 5a before forming 5b, and finally forming a third layer of oxide to cover 5a, 5b and the oxide layers previously formed to obtain the insulated electrodes structure of fig. 1 of '565.

Note additionally that it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchinson, 69 USPQ 138. Since the reset electrode as defined above has the ability to remove charges transferred to the reading diode (col. 2 ln. 43-46), the said reset electrode meets the claim limitation.

Note finally that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order

to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *See, e.g., In re Pearson, 181 USPQ 641 (CCPA)*; *In re Minks*, *169 USPQ 120 (Bd Appeals); In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). See MPEP §2114*. The recitation of "reading diode", "for converting into a voltage... shift register", "reset electrode", 'for emptying charges…" does not distinguish the present invention over the diode and electrodes of the prior art of Kamimura et al. in view of Kub that teaches the structure as claimed.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565) and Kub ('604) and further in view of Zoroglu ('535).

Kamimura et al. ('565) and Kub ('604) disclose all the limitations of claim 1 as stated above but do not appear to explicitly disclose using nitride as insulating layer above the doped polysilicon, leaving uncovered and covered portions of the doped polysilicon layer and oxidizing the doped polysilicon layer until a silicon pattern is obtained which comprises only the covered zones.

However Zoroglu ('535) discloses oxidizing polysilicon layer having covered (with a passivation layer) and uncovered portions to form electrodes (see Figs. 6-9 and column 4 line 23 through column5 lines 1-30 of '535).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have used silicon nitride as passivation layer and formed the doped polysilicon electrode according to the method of '535. One would have been

motivated to do so because silicon nitride is a commonly used passivation layer for electrodes in Microfabrication and the oxidation step would have avoided the etching step for removing uncovered portions of the doped polysilicon electrode.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565), Kub ('604), Zoroglu ('535) and further in view of Wolf (Silicon Processing for the VLSI Era, page 331).

Kamimura et al. ('565), Kub ('604) and Zoroglu ('535) disclose all the limitations of claim 2 as stated above but do not appear to explicitly disclose chemically attacking the unprotected portions of the doped polysilicon in order to remove it as much as possible before to oxidation step.

However Wolf discloses partially etching unprotected portions of a silicon layer before oxidizing (see page 331 of Wolf).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have partially etched the unprotected portions of the doped polysilicon before oxidizing the polysilicon layer. One would have been motivated to do so because doing so would have allowed the oxidized portions to have planar surface with the protected portions (see the first paragraph on page 331 of Wolf).

8. In view of the 112 rejection above, claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens ('990) and further in view of Kamimura et al. ('565).

Stevens disclosed an integrated circuit comprising a CCD register with a diode (formed by region 33 and substrate 26) at the end of the register, between a last electrode (16) of the register and a "reset" electrode (20), wherein the diode includes a doped region (33) delimited on one side by the last electrode and on the other side by region of thick silicon oxide (see Figs. 1-6 and 6, column 2 lines 44 through column line 68, column 4 line 63 through column 5 line 2 of '990), the doped region being entirely covered with a conductive layer 45 that is delimited according to a pattern which extends partly above the thick oxide 31 (figs. 3&6, col. 2 ln. 37-38 and col. 4 ln. 63-64) conductive layer 45 is delimited according to a pattern which extends partly above the thick oxide 31 (figs. 3&6, col. 2 ln. 37-38 and col. 4 ln. 63-64), and a conductive layer (gate electrode layer 40 above layer 45) entering in contact with the conductive layer 45 at a location not above the doped region (see figs. 3&5&6, col. 4 ln. 14-17). But Stevens ('990) does not appear to explicitly disclose the conductive layer 45 being polycrystalline silicon (it rather teaches aluminum in column 4 lines 63-64), an insulating layer covering the silicon pattern and having an opening not located above the doped region.

However, Kamimura et al. ('565) disclose a CCD interconnect structure consisting of an insulating layer covering a doped polycrystalline silicon pattern and having an opening not located directly above the doped contact region, and a conductive layer above the insulating layer and in contact with the silicon layer through the opening (see Fig. 1 and column 2 lines 26-63 of '565).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have used doped polycrystalline (instead of aluminum; the use

of polysilicon interconnect layer is well known in the art (see col. 2 ln. 52-54 and ln. 60-62 of '565), and as such, the use of conventional materials/components is obvious (see MPEP 2144.07)), covered the polycrystalline silicon pattern and made an opening not located directly above the doped contact region (see region where layers 40 and 45 contact on fig. 3 of '990), and to have formed the conductive layer (the gate 40) above the insulating layer to contact with the silicon layer through the opening in order to provide an interconnect structure (having an interlayer insulator between layers 45 and 40) for the device.

The Examiner notes that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See, e.g., *In re Pearson*, 181 USPQ 641 (CCPA); *In re Minks*, 169 USPQ 120 (Bd Appeals); *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). See MPEP §2114. The recitation of "reading diode", "readout diode", "reset electrode" "to convert into a voltage charges conveyed by the shift register" and "for emptying electrical charges received by the reading diode" does not distinguish the present invention over the prior art of Stevens ('990) in view of Kamimura et al. ('565) which teaches the structure as claimed.

See also the remark in claim 1 rejection above about the use of the language "adapted to".

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens ('990), Kamimura et al. ('565) and further in view of Spangler et al. ('064).

Stevens ('990) and Kamimura et al. ('565) disclose all the limitations of claim 4 as stated above but do not appear to explicitly disclose the polycrystalline layer covered with silicon nitride having the same pattern as the polycrystalline silicon, itself covered by an insulating layer and both nitride and insulating film having an opening located at the same position.

However, Spangler et al. ('064) disclose using nitride layer to cover doped polysilicon to prevent diffusion of impurities (see layer 160 on Fig. 5 and column 12 lines 50-64 of '064).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have covered the doped polycrystalline silicon pattern (in the device as per claim 4 rejection) with a silicon nitride layer, itself covered by the insulating film 8 and made a hole through both layers to allow contact with conductive layer 9 (see Fig. 1 of '565 and column 2 lines 53-62). One would have been motivated to do so to prevent impurities diffusion. Note that the nitride layer would have the same pattern as the polycrystalline silicon since the insulating layer it would replace as per claim 4 rejection above covers said polycrystalline according to the same pattern (see Fig. 1 of '565).

10. The prior art made of record and not relied upon are considered pertinent to applicant's disclosure.

Kim et al. (US 5,981,309) teach forming CCD image sensors with a diode having no contact hole above the conductive layer contacting the diode above the substrate surface..

Response to Arguments

11. Applicant's arguments filed on December 31, 2007 have been fully considered but they are not persuasive.

Applicants argued that the diode of ‘565 is not a reading diode and that the said diode has maximal size. This is not convincing because Applicants failed to demonstrate that the diode of '565 can not accomplish the function of the claimed diode and it is unclear what Applicants called "maximal size". The diode of '565 has the same structure as the claimed diode and there appears to be no contact opening directly above the doped region 33 and layer 45 where another contact is being made to layer 45. The region where conductive layer 40 (gate layer) contacts layer 45 is away from the region directly above doped region 33 as it is the case for the claimed invention.

Applicant’s argument about the “last electrode” is not convincing because the structure in the middle of fig. 1 of ‘565 is repeated and will stop at a certain point where the right most electrode would be the last electrode beyond which a different structure could be made. Moreover, "a last electrode" appears to depend on a given starting point

and a final point that can be arbitrary , and the rightmost electrode on fig. 1 of '565 is "a last" electrode going from the left. See also the remarks above regarding the "intended use" meaning conveyed by terms like "reading diode", "reset electrode" etc...

Applicant's argument regarding the contact of the reading diode being always made of Aluminum is not convincing because Aluminum is one of a limited number of conductive materials conventionally used to make interconnection structures in the Art of Microelectronic Fabrication, and these conventional materials also include doped polysilicon (see col. 2 ln. 53-55 and ln. 60-63 of '565 for example). As such, using doped polysilicon instead of Aluminum is obvious. There is nothing novel about using doped polysilicon as interconnect material.

Applicant's argument that Aluminum is not a functional equivalent of doped polysilicon is not convincing as per the preceding argument. Both are equivalent for the purpose of carrying electrical signals in interconnect structures and readily interchangeable in the art.

Applicant's argument about the patterned nitride not having the same pattern as the doped polysilicon is not convincing because the pattern of nitride, as per claim 5 rejection, would be present exclusively wherever the polysilicon is not oxidized into oxide as on fig. 11 of instant application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PENIEL M. GUMEDZOE whose telephone number is (571)270-3041. The examiner can normally be reached on M-T (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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